CLAIMS:

What is claimed is:

1. A method for testing the error handling capabilities of a system's firmware by allowing an analyzer to trigger on a specific system event, comprising:

defining a specific system event to be monitored;

creating a trigger in the analyzer, wherein the trigger is used to allow the analyzer to capture information related to the specific system event;

receiving a signal at the analyzer, wherein the signal automatically triggers the analyzer to capture and store a predetermined amount of data related to the specific system event before and after the trigger is executed.

2. The method of claim 1, wherein the signal is sent from one of a host system, a storage device, or a peer communications device.

3. The method of claim 2, wherein the signal is sent from a fibre channel host bus adapter in the host system.

4. The method of claim 1, wherein the analyzer is triggered within a millisecond of when the specific system event occurs.

5. The method of claim 1, wherein the specific system event is an error.

6. The method of claim 1, wherein the analyzer is an FC analyzer.

7. The method of claim 1, wherein the storage device includes initiators, targets, switches, or fabrics.

8. The method of claim 3, wherein the fibre channel host bus adapter includes a number of output pins, and wherein each output pin may be programmed with a separate triggering mechanism.

9. The method of claim 8, wherein the separate triggering mechanisms include detection of device errors above a certain threshold, device going away, illegal device activity, and input/output status.

10. A data processing system for testing the error handling capabilities of a system's firmware by allowing an analyzer to trigger on a specific system event, comprising:

defining means for defining a specific system event to be monitored;

creating means for creating a trigger in the analyzer, wherein the trigger is used to allow the analyzer to capture information related to the specific system event;

receiving means for receiving a signal at the analyzer, wherein the signal automatically triggers the analyzer to capture and store a predetermined amount of data related to the specific system event before and after the trigger is executed.

11. The data processing system of claim 10, wherein the signal is sent from one of a host system, a storage device, or a peer communications device.

12. The data processing system of claim 11, wherein the signal is sent from a fibre channel host bus adapter in the host system.

13. The data processing system of claim 10, wherein the analyzer is triggered within a millisecond of when the specific system event occurs.

14. The data processing system of claim 10, wherein the specific system event is an error.

15. The data processing system of claim 10, wherein the analyzer is an FC analyzer.

16. The data processing system of claim 10, wherein the storage device includes initiators, targets, switches, or fabrics.

17. The data processing system of claim 12, wherein the fibre channel host bus adapter includes a number of output pins, and wherein each output pin may be programmed with a separate triggering mechanism.

18. The data processing system of claim 17, wherein the separate triggering mechanisms include detection of device errors above a certain threshold, device going away, illegal device activity, and input/output status.

19. A computer program product in a computer readable medium for testing the error handling capabilities of a system's firmware by allowing an analyzer to trigger on a specific system event, comprising:

defining a specific system event to be monitored;

creating a trigger in the analyzer, wherein the trigger is used to allow the analyzer to capture information related to the specific system event;

receiving a signal at the analyzer, wherein the signal automatically triggers the analyzer to capture and store a predetermined amount of data related to the specific system event before and after the trigger is executed.

20. The computer program product of claim 19, wherein the signal is sent from one of a host system, a storage device, or a peer communications device.

21. The computer program product of claim 20, wherein the signal is sent from a fibre channel host bus adapter in the host system.

22. The computer program product of claim 19, wherein the analyzer is triggered within a millisecond of when the specific system event occurs.

23. The computer program product of claim 19, wherein the specific system event is an error.

24. The computer program product of claim 19, wherein the analyzer is an FC analyzer.

25. The computer program product of claim 19, wherein the storage device includes initiators, targets, switches, or fabrics.

26. The computer program product of claim 21, wherein the fibre channel host bus adapter includes a number of output pins, and wherein each output pin may be programmed with a separate triggering mechanism.

27. The computer program product of claim 26, wherein the separate triggering mechanisms include detection of device errors above a certain threshold, device going away, illegal device activity, and input/output status.